EECE696
Project Assignment 2
Due Tues 11/16/99 at COB

Introduction

Our primary work for the remainder of the semester is to design the KSU696 stereo FM transmitter IC and prepare it for fabrication on the Dec 27 AMI 1.2um process run. This is the first in a series of assignments that will guide you through the tasks needed. Directions for each team and team member are given below together with a list of 'deliverables' (things you must turn in) and an overview of the next assignment.

Grading for the three assignments will be based on the *completeness*, *correctness*, and overall *quality* of your work. Grading for the project portion of your total class scores will be 70% on your individual assignments and 30% on your company's final product.

The key to success for your company is for every team member to complete his/her work on schedule, and for the designs to be successful and robust. There is little or no duplication of effort in the assignments, so your company's success is critically dependent on you ! You are encouraged to work closely with others in your company and to seek help when needed, but your work on your assignments must, of course, be your own.

Chip Specifications and Design Considerations

A block diagram of the KSU696 IC has been previously passed out, together with your team assignment. The chip will be powered from a 5V ± 5% supply and should draw no more than 10 mA total current. It should be designed for high yield in the AMI 'ABN' process.

NOTE: The design rules for this process are being modified by MOSIS. The MOSIS web page no longer shows the AMI ABN process as 1.2um, but rather as a 1.6um process (lambda = 0.8u). This change was made recently by MOSIS after they determined that some analog circuits did not work well using the 1.2um rules. The web page states that designs at 1.2um (lambda=0.6u) will still be accepted, but for good yield, we should avoid making Fets with W < 4 lambda (min W of 6 lambda is recommended). Based on our own experience at 1.2um, I believe this will be sufficient, and working at 1.2um will allow our designs to be more compact. *Thus, we will use the ABN process at lambda=0.6u as we have done in all of our homework assignments.* Got to www.mosis.org and follow the links TechnicalSupport>FabProcesses>ABN for further info.

Team 1 - Digital Designers

Digital Designer A

Tasks:

- Design a ***static*** D flip-flop with asynchronous clear input and buffered clock input and Q and Q- outputs. It is recommended that you start with the basic CMOS D-latch discussed in class and add a clear input as described in the text. (See section 13.4) The buffer on the output is required to allow your flip flop to be connected to variable loads without changing any of its internal timing (setup and hold time, prop delays, etc.). Your buffer should be capable of driving approximately 5 unit loads. You should also include a clock buffer to avoid presenting more than one or two unit loads onto the clock line, and to minimize skew between the clk and clk- signals needed internal to your design.
- Draw a complete transistor level schematic of your flip flop labeling each fet and showing all transistor sizes (W and L).
- Estimate the performance of your design in terms of maximum toggle frequency. It is best to try to do this analytically, but you may run the simulator if you like (although we will need to simulate it later based on the circuit extracted from the layout to better model all parasitics). Our goal is to be able to use the flip flop in all portions of the design, so a toggle frequency of about 150 MHz is desired (100 MHz plus some margin). However, if we cannot hit 150 MHz, we can always design a simple dynamic flip flop later for the divide-by-8 portion of the KSU696 design.
- Create a layout of your flip flop in Magic. Your layout should follow standard ‘line-of-diffusion’ techniques, in a ‘standard-cell’ size/format agreed on by your company. See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.

Deliverables

- Full schematic (neatly drawn) with sizes of all Fets shown.
- Layout (printed and sent by email).
- Summary of predicted performance. Also include the size of layout to assist the test engineering in floorplanning.
- Appendix - Design notes

Preview of Next Assignment

- Plan a set of input waveforms to test functionality and characterize the device (in terms of prop delay, setup / hold times, etc.)
- Extract circuit from layout and run simulations. Fix design if needed.
- Repeat simulation for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models will be provided to do this.
- Draw block/schematic diagrams for divide-by-8 and S/P blocks needed in chip, and if necessary, design a dynamic flip-flop for the divide-by-8.

Digital Designer B

Tasks:

- Design a full adder circuit and a 2:1 digital MUX to be used in constructing an N-bit adder and counter (frequency divider) in future assignments. Review your notes, and section 12.4 of your text for info on these designs.
- Draw a complete transistor level schematic of your adder/mux, labeling each fet and showing all transistor sizes (W and L).
- Estimate the performance of your design in terms of worst case propagation delay. Note that the delay for the adder will be multiplied by up to 9 when we build the frequency dividers. Our goal is to be sure that the final 9-bit counter can run at 20 MHz (12.5 MHz required, plus some margin). It is best to try to estimate the propagation delay analytically, but you may run the simulator if you like (although we will need to simulate it later based on the circuit extracted from the layout to better model all parasitics).
- Create a layout of your adder/mux in Magic. Your layout should follow standard ‘line-of-diffusion’ techniques, in a ‘standard-cell’ size/format agreed on by your company. See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.

Deliverables

- Full schematic (neatly drawn) with sizes of all Fets shown.
- Layout (printed and sent by email).
- Summary of predicted performance. Also include the size of layout to assist the Test Engineer in floorplanning.
- Appendix - Design notes

Preview of Next Assignment

- Plan a set of input waveforms to test functionality and characterize the device (in terms of prop delay)
- Extract circuit from layout and run simulations. Fix design if needed.
- Repeat simulation for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models will be provided to do this.
- Draw block/schematic diagrams for counters and for the PFD (see Fig 18.1) and design/layout any additional gates needed to implement these designs.

Team 2 - Analog Designers

Analog Designer A

Tasks:

- Design a basic 2-input summing amplifier circuit for use in creating the stereo matrix. (see KSU696 block diagram) Choose a reasonable gain value that will not saturate the inputs of subsequent circuits (the goal here is summing, not necessarily amplification). Also, in biasing circuit, choose a reasonable bias current and provide 2.0V common mode levels at both the input and output. These voltage levels will allow direct coupling of circuits internal to the chip without the need for capacitors. (Remember however, that actual circuit voltages will vary due to circuit parameter tolerances, and it is not possible to cascade an arbitrary number of stages without some ‘DC restoration’ technique. Hopefully this will not be needed in our design...)
- Next, design a simple switching mixer for use in the AM modulator. It is recommended that you use the passive mixer topology (e.g. MUX based circuit) for which no biasing is needed.
- Finally, design the 3-input summer used in the modulator by adapting your summing amp above. You may want to be creative here, rather than just adding another diff amp to the 2-input summer. Remember that the 19kHz input signal is digital. This signal needs to be added in so that it is 10% of the L+R and L-R amplitudes, so you will need to reduce the amplitude substantially. Try to come up with a simple way of doing this.
- Draw complete transistor-level schematics of all your circuits, with sizes clearly shown.

Deliverables

- Full schematics (neatly drawn) with sizes of all Fets and DC bias voltages/currents shown.
- Explanation of pilot tone summing solution.
- An assessment of whether you think the circuit will still work if all process parameters (e.g. Vt, beta, Rsheet, etc.) vary independently by ± 15% during manufacturing.
- Appendix - Design notes

Preview of Next Assignment

- Create a spice circuit description of your circuits and simulate to check your bias points and overall functionality.
- Repeat simulation for 4 process corners (‘fast/slow’ nfets, and ‘fast/slow’ pfets). Additional spice models will be provided to do this.
- Create layouts for circuits after they are working well. (Your layout should follow standard ‘line-of-diffusion’ techniques in a ‘standard-cell’ size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.)

Analog Designer B

Tasks:

- Design a low frequency VCO with a nominal center frequency of 300 kHz and a voltage control range of at least ± 100 kHz. It is recommended that you use the circuit topology of Figure 18.8 in your text and that you read Section 18.1 carefully to understand how to design the comparator circuit. (A suggested target for the switching voltages is 2, 3 V or 1.5, 3.5V.) You should work with your teammate to establish what the nominal DC level will be at the output of his/her circuit, and what the peak AC signal level will be. This peak level should produce a frequency deviation of ± 75 kHz.
- Design a suitable capacitor using the area capacitance between poly and poly2 layers in the AMI process. Your goal here is to determine the physical size needed, and whether or not you need to make any changes to your circuit above. (Lowering currents should reduce the size of the C value needed if it is too large, as would increasing the comparator hysteresis.)
- After working out the basic design above, add a trim input circuit. You will need to be a little creative here. Your goal is to allow the center frequency of your oscillator to be adjusted when the final circuit is built using the KSU696 chip. This is typically done by having the board level designer attach a resistor to a pin on the chip, where the resistor (potentiometer) sets an internal current that adjusts the circuit. Provide a range of about ± 150 kHz.
- Draw complete transistor-level schematics of all your circuits, with sizes clearly shown.

Deliverables

- Full schematics (neatly drawn) with sizes of all Fets and DC bias voltages/currents shown.
- Explanation of trimming solution.
- An assessment of whether you think the circuit will still work if all process parameters (e.g. Vt, beta, Rsheet, etc.) vary independently by ± 15% during manufacturing.
- Appendix - Design notes

Preview of Next Assignment

- Create a spice circuit description of your circuits and simulate to check your bias points and overall functionality.
- Repeat simulation for 4 process corners (‘fast/slow’ nfets, and ‘fast/slow’ pfets). Additional spice models will be provided to do this.
- Create layouts for circuits after they are working well. (Your layout should follow standard ‘line-of-diffusion’ techniques in a ‘standard-cell’ size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.)

Team 3 - RF Designers

RF Designer A

Tasks:

- Sketch a Gilbert Cell mixer for use in ‘upconverting’ the LF VCO’s FM modulated signal to the transmitted frequency. Since the LF VCO is expected to be a digital signal (squarewave), feed this signal to the switching transistors of the Gilbert cell. The HF VCO signal should then be fed to the transconductor input, since it is expected to be a moderate amplitude analog sinewave.
- Work out your biasing solution for your Gilbert cell mixer by starting with a reasonable bias current and then determining what common-mode DC bias voltages need to be on the transconductor and switching cell transistors. The switching transistors can probably be directly coupled to an appropriate level shifter circuit (to be designed later in this assignment), so just decide what the bias V needs to be and assume the signal level will be a 0.5Vpk square wave centered on this value, but don’t worry about creating a bias V generator here. The transconductor portion of the design can be either AC or DC coupled to the HF VCO output. Work with your teammate to determine what you want to do there. My guess is that the HF VCO amplitude will be about 0.5Vpk for a half-circuit. Design your circuit accordingly, and provide a gain of about 1 so that the desired RF output signal will be about 0.25Vpk. (Recall that the sum and difference frequencies are each half the amplitude of the input)
- Design a circuit to convert the digital output of the LF VCO to a 0.5Vpk (half circuit) squarewave centered on the bias voltage assumed above. This will require a little creativity. Try to come up with a simple and robust (accurate bias V) solution.
- Draw complete transistor-level schematics of all your circuits, with sizes clearly shown.

Deliverables

- Full schematics (neatly drawn) with sizes of all Fets and DC bias voltages/currents shown.
- Explanation of how your LF VCO level shifter circuit works.
- An assessment of whether you think the circuit will still work if all process parameters (e.g. Vt, beta, Rsheet, etc.) vary independently by ± 15% during manufacturing.
- Appendix - Design notes

Preview of Next Assignment

- Create a spice circuit description of your circuits and simulate to check your bias points and overall functionality.
- Repeat simulation for 4 process corners (‘fast/slow’ nfets, and ‘fast/slow’ pfets). Additional spice models will be provided to do this.
- Create layouts for circuits after they are working well. (Your layout should follow standard ‘line-of-diffusion’ techniques in a ‘standard-cell’ size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.)

RF Designer B

Tasks:

- Design a high output impedance transconductor circuit to be used as the core of the HF VCO. This VCO will be implemented as a Gm-C based negative resistance oscillator as discribed in class notes, and the transconductor will be used to create the active inductor and the negative resistance circuits. For the latter, note that you will need to connect the transconductor output to the input, so consider this in your design when working out a biasing solution. (It should be possible to make this connection directly while keeping the transistors in the active region, but you may want to consider using a level shifter on the input to provide for more signal swing.)
- Design a common-mode feedback circuit (CMFB) to stabilize your transconductor's high impedance output nodes at an appropriate bias voltage. Review the class notes on this circuit, and work out the reference voltage needed to maintain the CM voltage of your transconductor at an appropriate value. It is recommended that the two Nfets used in the common-mode summer (the source followers at the CMFB input) have moderate W/L values and the Pfets used to form the differential comparator circuit have a very large W/L ratio. This will help guarantee that the bias solution will depend primarily on the Vt of the FETs used, and will provide high gain in the comparator.
- Draw complete transistor-level schematics of all your circuits, with sizes clearly shown.
- Do preliminary simulations on your circuit to check that your CMFB design works.

Deliverables

- Full schematics (neatly drawn) with sizes of all Fets and simulated DC bias voltages/currents shown.
- An assessment of whether you think the circuit will still work if all process parameters (e.g. Vt, beta, Rsheet, etc.) vary independently by ± 15% during manufacturing.
- Appendix - Design notes

Preview of Next Assignment

- Simulate to check your circuit's transconductance and output resistance values (using an AC analysis with an AC voltage of 1.0 applied to the HF VCO port to check gm, and then using an AC current source of 1.0 applied at the drains to check the output resistance).
- Implement the full HF VCO by using your transconductor to create the negative R and active L circuits and document in the form of a schematic/block diagram. Your should be able to provide the frequency adjustment control by controlling the bias currents that affect gm (and hence the active L value).
- Simulate your oscillator to check functionality and then repeat simulations for 4 process corners ('fast/slow' nfets, and 'fast/slow' pfets). Additional spice models will be provided to do this.
- Create layouts for circuits after they are working well. (Your layout should follow standard 'line-of-diffusion' techniques in a 'standard-cell' size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.)

Team 4 - Test Engineer

Tasks:

- Go to the MOSIS web site and get information on the IC package that we will use in our chip. We need to know which pins on the chip correspond to which pads in the chip. You should be able to find this information by following the links Products>PackagingOptions>PackagesAvailableThroughMOSIS and then looking at the 40 pin DIP package. (This is the only option available to us since we are fabbing under an educational account.) Print the package and bonding diagrams for later reference.
- Go to the class web page and download all of the padframes and pads. Then examine each cell in magic and document it. As a minimum, you should describe what the cell is for and what connections it has (Is it an input, output, power, or ground pad? If an input or output pad, does the signal that goes to the chip circuit connect directly to the pad, or through circuitry? What kind of circuits and why?)
- In our chip we will need to use a combination of analog and digital I/O pads. The pad frames provided on the web page only contain one type or the other. Practice creating a modified pad frame with both pad types. This can be done either in magic (being careful to position the pads accurately when swapping them out), or by directly editing the '.mag' file (which is in ascii form and you can probably figure out well enough to make the changes needed).
- Study the block diagram of our chip and do a preliminary floorplan (positioning of different teams circuits into specific location inside the pad frame) and assignment of signals to pads and package pins. With 40 pins, we will hopefully have many left over after assignment. These will be used to add test points into the design so that if something doesn't work, we can try to find out what went wrong. (Assignment of test points to pins will be done in the next project assignment.) In floorplanning and signal assignments, remember that analog and digital signals should be separated to prevent crosstalk. Also, note that the analog and digital Vdd and Ground signals should be on separate pads/pins. Generally, the corner pads are used to supply pwr/gnd to digital circuits (and the associated pads), while other pwr/gnd pads may be inserted into the frame for the analog circuits. There are no simple rules to work out the best solution for minimizing crosstalk. Give this issue a lot of thought and try to come up with a good solution...

Deliverables

- Printouts of package and bonding diagram
- List of pads and description (see directions above)
- Printout of your modified pad frame with mixed analog and digital I/O pads
- Preliminary flooplan and signal list assigning signals to package pins and pads in the pad frame.

Preview of Next Assignment

- Get schematics from other teams, analyze them to understand the circuits that will be used in the chip, and estimate the area consumption on the die required by each teams circuits.
- Identify the test points needed to troubleshoot the design if there is an error when when we get the chip back. The goal would be to locate the offending circuit(s), and if possible, provide a workaround.
- Design any buffering/MUX circuits needed to support placing test points in the chip.
- Design a board-level test circuit for use in chip testing/troubleshooting.