EECE696
Project Assignment 3
Due Tues 11/30/99 at COB

Introduction

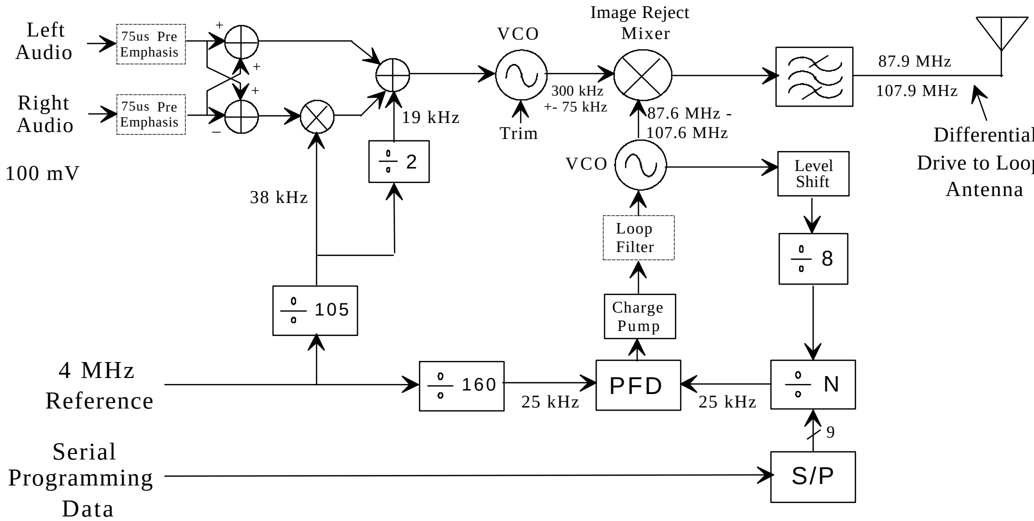
This is the second in a series of assignments designed to guide you through the design of the KSU696 IC. The main goals of this assignment are to test and refine our previous circuits, and to use these basic circuits as cells to build the principle blocks needed (counters, oscillators, PLLs, etc.). As before, specific tasks and deliverables are given in this assignment for each engineer, and a preview of the next assignment is provided.

As you work on your designs, you should keep in mind that everyone's layouts must fit in the allocated space within the IC (approx 1.5mm x 1.5mm excluding the pads). *Work with your team and company personnel (esp. the layout/test engineer) to plan ahead on where your circuits will be placed in the final die, and to plan for testing the circuits after they are fabricated.*

Also, to add more realism to the project, we will look at *yield* issues in this assignment. Your instructor has placed additional spice models on the course web page that can be used to simulate your designs over the range of values typically encountered for threshold voltages, transconductances, and capacitances. If your design works for all of these models (there are four 'corners', plus the nominal values), then you can expect that it will be manufacturable.

Revised Block Diagram

The latest revision of the chip block diagram is shown below. It is also available now on the course web page.



KSU696

Monolithic Stereo FM Broadcast Band Transmitter

Rev 1.2

Team 1 - Digital Designers

Digital Designer A

Tasks:

- Plan a set of input waveforms to test functionality and characterize the flip flop you designed in the previous assignment. As a minimum, you should run simulations that will allow you to be certain your flip-flop is functional (including the async clear input), and to determine the propagation delays (clock-to-Q and clock-to-Qbar for both transitions, the setup time, and the propagation time from Clear to Q and Qbar).
- Extract circuit from layout, run the simulations needed, and record the results in a tabular format.
- Repeat simulation for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models are provided on the class web page to do this.
- Check your manufacturability further by determining which models gave the worst case performance and then using this models at other temperatures. Add a '.options temp = 70' line to your circuit description to specify a temperature of 70 C, which should be the worst case. Then repeat for a temperature of -20 C.
- Determine if the flip flop is fast enough to use in the divide-by-8 circuit, and if necessary, design, layout, and test a dynamic flip flop for this block of the chip.
- Draw block/schematic diagrams for divide-by-8 and S/P blocks needed in chip.
- Plan the layout of these blocks, drawing your flip flops as rectangles, and showing all connections needed between them. This will be used as a guide in the next assignment where you will place the flip flops as cells, connect them, extract the final circuits, and check their operation.

Deliverables

- An explanation of the tests you did (including drawings or printouts of the waveforms you used).
- A tabular summary of your device's performance with nominal models.
- A summary of worst case performance over all process corners and temperature.
- Your assessment of whether you can achieve the maximum toggle speed, and documentation of the dynamic flip flop (schematic/layout/simulations) if you needed to create one.
- Block diagrams for how you will create your divide-by-8 and S/P blocks.
- Your planning drawing for layout of these blocks.

Preview of Next Assignment

- Work with the VCO designer to implement a level-shifter that can be used to connect his/her output to your divide-by-8 block.
- Meet with your team to make final decisions on placement and routing of your circuits.
- Layout the divide-by-8 and S/P blocks.
- Extract and simulate these blocks to verify their functionality (this is essentially what industry calls 'LVS' (layout versus schematic check).
- Check the performance of these circuits.
- Work with the test engineer to add test points to your circuit.

Digital Designer B

Tasks:

- Plan a set of input waveforms to test functionality and characterize the full adder and mux you designed in the previous assignment. As a minimum, you should run simulations that will allow you to be certain your circuits are functional for all 8 input combinations, and to determine the worst case adder propagation delays (low to high and high to low transitions) from inputs and carry in to sum out and carry out, and the propagation delay through the mux.
- Extract your circuit from the layout done in the past assignment, run the simulations needed, and record the results in a tabular format.
- Repeat simulation for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models are provided on the class web page to do this.
- Check your manufacturability further by determining which models gave the worst case performance and then using this models at other temperatures. Add a '.options temp = 70' line to your circuit description to specify a temperature of 70 C, which should be the worst case. Then repeat for a temperature of -20 C.
- Get the flip flop layout and propagation delay data from your teammate.
- Draw block/schematic diagrams for div-by-N circuit needed in the chip. Then draw block/schematic diagrams for the div-by-105 and div-by-160 circuits (These should be easy after the div-by-N is done. Just preset the N value on the more general circuit).
- Using your propagation delay data and that from your partner, determine if your div-by-N circuit is fast enough.
- Plan the layout of these blocks, drawing your flip flops and adders/muxes as rectangles, and showing all connections needed between them. This will be used as a guide in the next assignment where you will place the flip flops as cells, connect them, extract the final circuits, and check their operation.

Deliverables

- An explanation of the tests you did (including drawings or printouts of the waveforms you used).
- A tabular summary of your device's performance with nominal models.
- A summary of worst case performance over all process corners and temperature.
- Block diagrams for how you will create your counters.
- Your assessment of whether you can achieve the speed needed in the div-by-N counter.
- Your drawing for the planned layout of these blocks.

Preview of Next Assignment

- Design and layout the PFD circuit and work with the VCO designer to implement a charge pump circuit that connects your PFD output to his/her VCO input.
- Meet with your team to make final decisions on placement and routing of your circuits.
- Layout the counters and the charge pump.
- Extract and simulate these blocks to verify their functionality (this is essentially what industry calls 'LVS' (layout versus schematic check).
- Check the performance of these circuits.
- Work with the test engineer to add test points to your circuit.

Team 2 - Analog Designers

Analog Designer A

Tasks:

- Work with your teammate to be sure your circuit interfaces properly to the LF VCO input.
- Create spice circuit descriptions of your summer circuits and simulate to check your bias points. (You may want to use subcircuits to modularize your work.)
- Check the overall functionality of all of your circuits. For the summers at the input of the chip, use capacitive coupling and input sinewaves at two different frequencies to the two different inputs so you can be sure it is working properly. Do the same for the output summer, but with the 19 kHz squarewave also. Are the relative amplitudes correct? Note that you can probably safely omit simulations for the mixer. It should work fine if it is the correct topology, and it will be checked later after layout.
- Repeat simulation for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models are provided on the class web page to do this. If you have any resistors in your circuit, vary these by +- 15% too to be sure everything will work.
- Check your manufacturability further by determining which models gave the worst case performance and then using these models at other temperatures. Add a '.options temp = 70' line to your circuit description to specify a temperature of 70 C, which should be the worst case. Then repeat for a temperature of -20 C.
- Create layouts for your circuits after they are working well. Your layouts should follow standard 'line-of-diffusion' techniques in a 'standard-cell' size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.

Deliverables

- Copies of your spice circuit description files.
- An assessment of how well your bias points matched design values
- Descriptions of the transient analysis simulations you ran and plots of the outputs confirming correct functionality of the three summers.
- A summary of your process corner checks. Did your circuit work for all 4 corner models? Does it work over temperature too?
- Circuit layouts (printed and sent to me by email (with a .gif suffix)).

Preview of Next Assignment

- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Meet with your team to make final decisions on placement and routing of your circuits.
- Work with the test engineer to add test points to your circuit.

Analog Designer B

Tasks:

- Work with your teammate to be sure your frequency control input interfaces properly to the summer output.
- Create spice circuit descriptions of your circuit. You should create the comparator as a subcircuit so that it can be simulated independently.
- Simulate the comparator circuit using a transient analysis so that you can test its speed as well as its switching points. For this, you will need to use a squarewave input with slow rise and fall times (e.g. 50 ns).
- Simulate the overall functionality of all of your oscillator. You should use a step source on Vcc (zero volts initially, then rising to 5V in a us or so) so that the simulator can converge to an intial solution. Then, as time progresses, and the step on Vcc occurs, you can see the full startup of your oscillator. Does it work as expected? Is the nominal frequency correct? Do you have the proper frequencies for different control voltages? Does your trim adjustment have the proper range?
- Repeat critical simulations (e.g. the nominal frequency case) for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models are provided on the class web page to do this. If you have any resistors in your circuit, vary these by +- 15% too to be sure everything will work.
- Check your manufacturability further by determining which models gave the worst case performance and then using these models at other temperatures. Add a '.options temp = 70' line to your circuit description to specify a temperature of 70 C, which should be the worst case. Then repeat for a temperature of -20 C.
- Create layouts for your circuits after they are working well. Your layouts should follow standard 'line-of-diffusion' techniques in a 'standard-cell' size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.

Deliverables

- Copies of your spice circuit description files.
- An assessment of how well your switching points matched the planned values and what your comparator speed is.
- Descriptions of the transient analysis simulations you ran and plots of the outputs confirming correct functionality and frequencies of operation of the oscillator.
- A summary of your process corner checks. Did your circuit work for all 4 corner models? Does it work over temperature too? Is the trim range sufficient?
- Circuit layouts (printed and sent to me by email (with a .gif suffix)).

Preview of Next Assignment

- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Meet with your team to make final decisions on placement and routing of your circuits.
- Work with the test engineer to add test points to your circuit

Team 3 - RF Designers

RF Designer A

Tasks:

- Create a spice description of your circuit.
- Simulate the mixer in a DC mode first to check the bias points. For the LF VCO input, you should set the value first to 0 and then to 5V, which will allow you to check that your level shifter circuit is working correctly (converts these levels to the correct offset and the 0.5Vpk change at the mixer switching fet gates).
- Next, check the frequency response of the differential amplifier with the switching transistors held in one state (0 or 5V). In this state, two of the switching fets are on and two are off. Those that are on act as cascoding transistors, passing the diff amp output to the load resistors (active or passive). We want to input an ac signal (AC 1.0) to the diff amp and check the frequency response to the load resistors. If all is well, the gain will be about 1 (see previous assignment), and the corner frequency will be > 100 MHz.
- Next, simulate in a transient analysis mode to check the mixing operation. You should input a suitable squarewave at the LF VCO input, and a sinewave at the HF VCO input. Check with your teammate to determine the correct signal level and bias offset to use for the HF input. You may want to use frequencies of 10 MHz and 11 MHz and simulate for about 2us. This will allow you to see the sum and difference frequencies produced at the output better than if you use the actual frequencies we expect to use.
- Repeat critical simulations (e.g. the bias point and frequency response checks) for 4 process corners (fast/slow nfets, and fast/slow pfets). Additional spice models are provided on the class web page to do this. If you have any resistors in your circuit, vary these by +- 15% too to be sure everything will work.
- Create layouts for your circuits after they are working well. Your layouts should follow standard 'line-of-diffusion' techniques in a 'standard-cell' size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse.

Deliverables

- Copies of your spice circuit description files.
- An assessment of how well your DC bias points matched design values, and of your level shifter operation.
- Descriptions of the AC and transient analysis simulations you ran and plots of the outputs confirming correct functionality.
- A summary of your process corner checks. Did your circuit work for all 4 corner models?
- Circuit layouts (printed and sent to me by email (with a .gif suffix)).

Preview of Next Assignment

- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Meet with your team to make final decisions on placement and routing of your circuits.
- Work with the test engineer to add test points to your circuit

RF Designer B

Tasks:

- Simulate your transconductor circuit to check the gm value. This can be done by running in an AC analysis mode (from 10 MHz to 1 GHz) with an AC voltage of 1.0 applied between the inputs (‘vin inplus inminus 0.0 ac 1.0’), placing a zero valued voltage source in series with the drain of one transistor in the diff amp, and plotting the current. Since the input V is 1.0, the current will be the gm value. Use the value at 100 MHz and confirm that your circuit’s corner frequency is at least this high.
- Review the class notes on how to implement the active inductor circuit and the negative resistor circuit, and then draw a schematic for a negative resistance oscillator circuit implemented from these elements. (You will need three transconductors and two capacitors, where one C is inside the active L circuit and the other is the C of the RLC oscillator circuit). Don’t draw all the transistors that make up the three transconductors you will use. Just draw each transconductor as a block with differential inputs and outputs.
- Add blocks showing CMFB circuits needed. Note that only two are needed, since the output of the negative R transconductor connects to one of the transconductor outputs in the inductor.
- Select values for the capacitors, based on the gm value you found in the first step. One choice is to select X_C in the inductor to be equal to 1/gm, and then choose the C in the RLC circuit to set the frequency to the correct value.
- Modify your circuit description for the transconductor by separating out the CMFB and gm circuits and making each one a subcircuit. Then use these subcircuits to build up a simulation file for the complete oscillator.
- Simulate the oscillator in a transient analysis mode. You should use a step source on Vdd to allow the simulator to reach convergence at time zero. Is the frequency correct? Is the amplitude as expected? If you need to adjust the frequency, change the C values as needed.
- Note that the inductance value depends on gm, and that gm can be varied by varying the ‘tail current’ (if the transconductor transistors are operating in the long-channel regime). Use this fact to vary your oscillation frequency by modifying your current sources on the inductor transconductors to be externally controlled, and see if you can get a sufficient frequency range (according to the math, variation of +-15% in gm should vary L by +-30% and hence, frequency by +-15%, but this will probably require at least a +-30% change in current.).
- Create layouts for your circuits after they are working well. Your layouts should follow standard ‘line-of-diffusion’ techniques in a ‘standard-cell’ size/format agreed on by your company (as far as practical). See chapter 15 for more info. Also, use hierarchy where appropriate to enhance modularity, maintainability, and reuse. **NOTE If you run out of time to do this, just plan the layout and implement it in the next assignment**.

Deliverables

- Simulation file and plot from gm simulation, and assessment of gm value and corner frequency.
- Schematic of full oscillator (with gm and CMFB circuits shown as blocks and capacitors and gm blocks shown with their values).
- Simulation file and plot from your full oscillator, and an assessment of what the frequency of oscillation is.
- Plots from varying the tail current, and what the frequencies you can achieve are.
- Circuit layouts (printed and sent to me by email (with a .gif suffix)) if you made it this far...

Preview of Next Assignment

- Complete the layout and then extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry.

Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.

- Meet with your team to make final decisions on placement and routing of your circuits.
- Work with the test engineer to add test points to your circuit

Team 4 - Test Engineer

Tasks:

- Get schematics from other teams and analyze them to understand the circuits that will be used in the chip.
- Identify the test points needed to troubleshoot the design if there is an error when we get the chip back. The goal would be to locate the offending circuit(s), and if possible, provide a workaround. Note that there will generally be more test points desired than can be accommodated. One solution is to design MUX circuits on the chip. Another option is to put copies of these circuits onto a second chip (we can make two designs per company). Discuss these options with your company and decide on what you want to do.
- Design any buffering/MUX circuits needed to support placing test points in the chip and work with your company's teams to be sure these will not load their circuits excessively.
- Estimate the area consumption on the die required by each teams circuits and work with your team to help them plan the final layouts. Generate revised floorplans and distribute them to your company as you continue to get layouts submitted to you.
- Generate the pad frame that you will use, based on your revised floorplans and any changes you need to make in your pin list from the first assignment.
- Design a board-level test circuit for use in chip testing/troubleshooting. Start by drawing a schematic, and then do a preliminary board layout. We have Microsim's 'PCBoards' program for doing layouts. You can practice with this tool using version 8 of the Pspice evaluation program.

Deliverables

- A complete set of the most recent versions of your company's schematics
- A listing ***and justification*** of the test points you plan to use. Show them on the schematics and on the block diagram using a red pen or yellow marker to highlight them.
- A description of any buffer/MUX circuits you plan to use, and schematic(s) for these circuits.
- Your revised floorplan and your pad frame. (email me the latter)
- A schematic of your board-level test circuit(s), together with a hand sketched PC board layout.

Preview of Next Assignment

- Create a final floorplan, and head up the layout of the full chip. You should work closely with your company's teams to begin placing their designs into the pad frame as early as possible.
- Work with your company to check the layouts carefully. Use the 's' command in Magic to trace connectivity from each pad to the appropriate circuit, and to verify that there are no shorts (espectially between power and ground !)
- Do a layout of the board-level test circuit(s).
- Create your company's 'signature' layout.