

EECE696

Project Assignment 4

Due Thurs 12/9/99 at COB

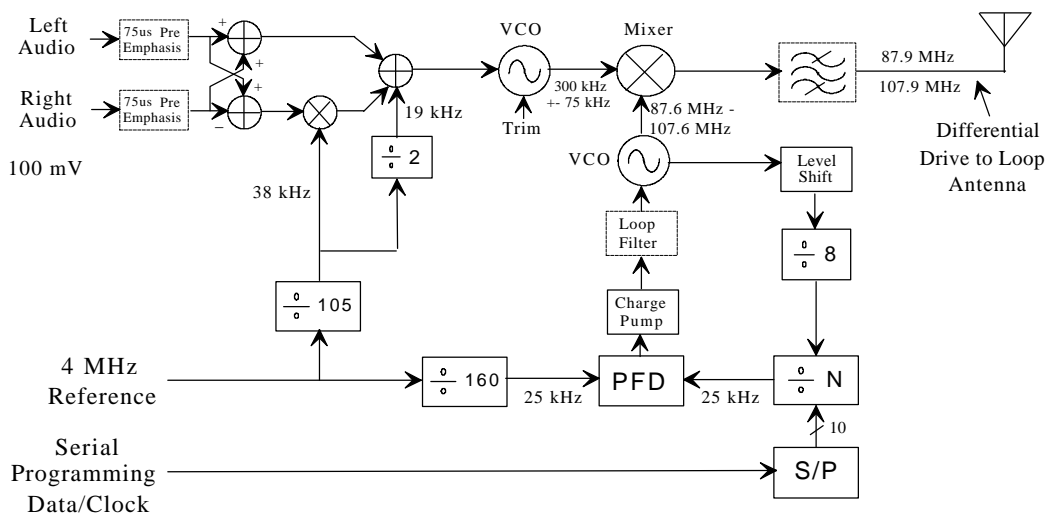
Introduction

This is the third (and final) in a series of assignments designed to guide you through the design and testing of the KSU696 IC. The main goals of this assignment are to finalize your layouts, to verify them by extracting your circuit and running simulations on the extracted spice file, and to prepare everything for integration into your company's chip(s). As before, specific tasks and deliverables are given in this assignment for each engineer, and a preview of the next assignment is provided.

It is important that you complete this assignment on-time so that studying for your exams is not impacted. Also, we need to have layouts ready for integration into the full chip. This integration is tentatively scheduled for Friday or Saturday, 12/10 or 12/11.

Revised Block Diagram

The latest revision of the chip block diagram is shown below. Note that the width of the S/P register and of the divide-by-N counter has been changed from 9 to 10. Also, the bandpass filter has been shown in dashed lines to indicate that it will not be implemented in this prototype.



KSU696

Monolithic Stereo FM Broadcast Band Transmitter

Rev 1.3

Team 1 - Digital Designers

Digital Designer A

Tasks:

- Work with the VCO designer to implement a level-shifter that can be used to connect his/her output to your divide-by-8 block. The VCO output is a sinewave, centered on a DC bias. Most likely, this bias is not the same as the switching point of your divide-by-8, so that the output needs to be level shifted. In addition, the output amplitude may be too low to reliably drive your flip flop. If this is the case, design a small amount of gain (what ever is needed for reliable operation) into your level shift.
- Layout the level shifter and your divide-by-8 and S/P blocks.
- Extract and simulate these blocks to verify their functionality (this is essentially what industry calls 'LVS' (layout versus schematic check)).
- Check the performance of these circuits. To minimize your workload, you can just simulate with the nominal device models and with the models that gave you worst case performance previously.
- Work with the test engineer to add test points to your circuit, and to guarantee that these test points do not load your circuit.
- Prepare your layouts for integration with the rest of your company's chip.

Deliverables

- A schematic of your level shifter circuit, with a brief explanation of its design and operation.
- Your layouts (printed and send via email with a .gif suffix).
- Simulation plots verifying the layouts of the level-shifter/divide-by-8 combination, and of the S/P register.
- A summary of the level-shift/divide-by-8 circuit's performance determined from your simulations.

Digital Designer B

Tasks:

- Review and then draw a schematic for the PFD circuit. This is basically Figure 19.10 in your text, but you may want to put a few inverters in series between the output of the AND gate and the clr input of the flip-flops. If you don't, there may be a race condition.
- Design a charge pump circuit like that in Figure 19.12. Use current sources of about 500uA, and make sure the circuit can drive current into a capacitor for any capacitor voltage between about 1V and 4V. Note that the FETs M1, M2 in this circuit act as simple switches and are in the triode region when on. Hence, they should be relatively large to provide a low on-resistance.
- Get a static D flip-flop from your teammate and layout the PFD and the charge pump circuits.
- Create layouts for the counters (frequency dividers) needed in the chip, based on the block diagrams you created in the previous assignment. Use the static D flip flop from your teammate.
- Extract and simulate these circuits to verify their functionality (this is essentially what industry calls 'LVS' (layout versus schematic check)).
- Verify the performance (speed) of the programmable counter circuit. To minimize your workload, you can just simulate with the nominal device models.
- Work with the test engineer to add test points to your circuit, and to guarantee that these test points do not load your circuit.
- Prepare your layouts for integration with the rest of your company's chip.

Deliverables

- Schematic of your combined PFD and charge pump circuit.
- Your layouts (printed and send via email with a .gif suffix).
- Simulation plots verifying operation of the PFD/charge-pump circuit layouts.
- Simulation plots verifying operation of the counter circuit layouts.
- A summary of the counter circuit performance (maximum frequency of operation) determined from your simulations.

Team 2 - Analog Designers

Analog Designer A

Tasks:

- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Check the bias voltages throughout your circuit against those you simulated previously to be sure all FETs are properly drawn.
- Check the overall circuit functionality using the same input waveforms you used in your design.
- Work with the test engineer to add test points to your circuit, and to guarantee that these test points do not load your circuit.
- Prepare your layouts for integration with the rest of your company's chip.

Deliverables

- A table comparing the bias voltages from the extracted circuit against those of the previous assignment's simulations.
- Simulation results verifying proper overall operation of the extracted circuit and comments on whether these match the design.

Analog Designer B

Tasks:

- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Check the bias voltages in your voltage controlled current source against those you simulated previously to be sure all FETs are properly drawn.
- Check for proper extraction of the capacitor and modify this in the spice file if needed.
- Check the overall circuit operation.
- Meet with your team to make final decisions on placement and routing of your circuits.
- Work with the test engineer to add test points to your circuit, and to guarantee that these test points do not load your circuit.
- Prepare your layouts for integration with the rest of your company's chip.

Deliverables

- A table comparing the bias voltages from the extracted circuit against those from the simulations run in the previous assignment.
- Simulation results verifying proper overall operation of the extracted circuit and comments on whether these results match those from the previous assignment.

Team 3 - RF Designers

RF Designer A

Tasks:

- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Check the bias voltages throughout your circuit against those you simulated previously to be sure all FETs are properly drawn.
- Check the overall circuit operation using the same waveforms/procedure used in the design.
- Work with the test engineer to add test points to your circuit, and to guarantee that these test points do not load your circuit.
- Prepare your layouts for integration with the rest of your company's chip.

Deliverables

- A table comparing the bias voltages from the extracted circuit against those of the simulations from the previous assignment.
- Simulation results verifying proper overall operation of the extracted circuit and comments on whether these match those of the previous assignment.

RF Designer B

Tasks:

- Work with the digital design team to be sure your circuits input and output voltage levels interface properly to their circuits (charge pump and level-shifter).
- Complete the layout of your circuit.
- Extract a circuit description from your layout and simulate to be sure your layout matches the schematic. This is called layout-vs-schematic (LVS) checking in industry. Note that resistors do not extract properly, so you will have to 'patch up' your extracted circuit in these areas. To do this, make a copy of your layout, delete the resistors, and then name the nodes where the two ends of the resistor attach. This will help you locate the place in the schematic where you need to add the resistors back in after extraction.
- Check for proper extraction of the capacitors and modify these in the spice file if needed.
- Check the overall circuit operation.
- Work with the test engineer to add test points to your circuit, and to guarantee that these test points do not load your circuit.
- Prepare your layouts for integration with the rest of your company's chip.

Deliverables

- Circuit layout (printed and sent to me by email (with a .gif suffix)).
- Simulation results verifying proper operation of the extracted circuit and comments on whether these match the design.

Team 4 - Test Engineer

Tasks:

- Create a final floorplan for the full chip(s) your company will produce. Draw your company's floorplan(s) to-scale, showing and labeling each team/individual's blocks. (Be sure to include room for the chip 'signature'.)
- Create a final pinout listing, including test points.
- Create a layout of your company's 'signature' and add this to the design. Work with your company to decide if you want just a company name, or designer names, initials, etc. How about a KSU power cat??
- Create layouts of any buffer and MUX circuits needed, and extract these circuits and simulate them to verify their functionality. It is recommended that you create at least an analog buffer (either a simple source follower amp, or a unity gain buffer configured opamp), and an analog/digital mux (8:1 or 16:1) - even if these circuits are not strictly required by the available pins on the chip. This is your main opportunity to place some circuits on the chip!
- Do a layout of the board-level test circuit(s) using PC Boards software.

Deliverables

- Final floorplan diagram.
- Table of pin assignments.
- Signature layout.
- Schematics and layouts of any buffer/MUX circuits you used, together with simulation results verifying operation of the buffer/MUX circuits.
- Final schematic and layout of your board-level test circuit(s).