

EECE 696
Integrated Circuit Design
Fall 1999

Instructor: Bill Kuhn
265 Rathbone Hall

Office Hours: TU 2:30 - 5:20 (except during bi-weekly Thursday faculty meetings).
Others by appointment

Prerequisites: Electronics I (EECE525) and Intro to Computer Engineering (EECE241), or equivalent.

Text: Baker, Li, and Boyce, "CMOS Circuit Design, Layout, and Simulation," c. 1998, IEEE Press.

Objectives: This course covers the fundamentals essential to understanding the design and performance of modern integrated circuits. Emphasis is placed on CMOS ICs, which account for approximately 80% of all ICs produced by industry today. CMOS is used in implementing processors such as the Intel Pentium™, microcontrollers, and memory chips, and is beginning to be used in many analog and mixed-signal (analog/digital) products as well.

At the conclusion of the course, you will be able to:

- Understand the basic building blocks used in digital and analog ICs
- Understand the fundamentals of IC fabrication
- Understand the performance capabilities and limitations of modern CMOS submicron technologies
- Use Electronic Design Automation (EDA) tools for layout and simulation of circuits
- Create "full-custom" designs of small to medium scale analog and digital circuits

Project: A major feature of the course will be a class design of a significant mixed-signal (digital + analog) integrated circuit. Students will be divided into two competing 'companies', with each company split into teams that will work on sections of their company's IC product. Each team will progress through the standard IC design phases of circuit definition, simulation, layout, and layout verification. The teams will also need to coordinate with other members of the company on signal interfaces, chip 'floorplanning', test planning, and final integration of all designs into a single IC 'die'. Assuming these tasks are completed successfully, the completed designs will be submitted to the MOSIS service to be fabricated, and completed parts will be available for testing approximately 12 weeks later.

Computer Use: The EDA tools used in this course will include ‘Magic’ for IC layout, and ‘Spice3’ for circuit simulation. These are standard tools used by schools throughout the country and are the same tools used by universities in the heart of Silicon Valley (e.g. Stanford).

You will need to get a computer account on the department’s system if you do not already have one. Loleita in the front office should have the forms.

Additional: You will need a package of colored pencils since IC layouts involve top-views of many stacked layers. Your professor will use colored chalk from time-to-time when needed to make these layouts easier to follow on the board and the colored pencils will help you in your note taking, as well as in doing draft layouts on paper for the project.

Costs: The fabrication of integrated circuits is an expensive undertaking (approx \$1000 to \$50,000 for a prototype chip depending on size and other factors). However, all of this cost is being covered by MOSIS, the National Science Foundation, and by interested IC fabrication companies (currently American Microsystems Inc. (AMI) and Hewlett Packard (HP)).

To guarantee that this money is well spent, we must design functional circuits, simulate them thoroughly before sending the designs for fabrication, and have a test plan and one or more individuals take on the responsibility for testing when the chips are returned to us next semester. Your professor will only send chips to be fabricated if all of these conditions are met.

Grading: Your grade will be based on the following breakdown:

- Homework 30% (lowest one dropped)
- Midterm 20%
- Final 20%
- Project 30%

Disabilities: If you have any condition, such as a physical or learning disability, which will make it difficult for you to carry out the work as outlined or which will require academic accommodations, please notify me in the first two weeks of the course.

The All-New Kansas State University Honor Code:

Beginning Fall 1999, KSU is instituting a new honor code system. The essentials are stated below. Please see www.ksu.edu/honor to learn more.

The Honor System is defined by the following Code:

- a. That as K-State students they will not give or receive aid in examinations; that they will not give or receive unpermitted aid in class work, in the preparation of reports or in any other work that is to be used by the instructor as the basis of grading.
- b. That as K-State students they will do their share and take an active part in seeing to it that others as well as themselves uphold the spirit and letter of the Honor System. This includes reporting an observed dishonesty.

The Honor Pledge Statement

On all course work, assignments, or examinations done by students at Kansas State University, the following pledge is either required or implied:

On my honor as a student I have neither given nor received unauthorized aid on this assignment.

This statement means that the student understands and has complied with the requirements of the assignment as set forth by the instructor

EECE696 Integrated Circuit Design
Course Topics (Tentative)

Week	Topics	Reading
1	History of the IC, Intro to CMOS The IC design cycle and EDA tools	Preface Sect 1.1 and 1.3
2	IC Fabrication and IC layouts UNIX review and Intro to Magic	Chap 2 Handouts
3	Simulation with Spice and Irsim IC packaging, pad frames, and metal interconnects	Class notes Sect 3.1 - 3.3
4	MOSFETs - Layout, fab, parasitics MOSFETs - Device physics, IV curves	Chap 4 Chap 5 (skim Sect 5.2)
5	MOSFETs - Device physics, IV curves continued Analog and Digital MOSFET models	Chap 5 (skim Sect 5.2) Chap 9 and 10
6	Digital circuits - delay, power consumption, latchup Gates - Nand, Nor, Complex, Xor, Adders, Tristate Buffers	Chap 11 Chap 12
7	Flip flops System level block examples (Shift regs, N-bit adders, counters, multipliers)	Chap 13 Class notes
8	<u>Midterm Exam</u> -- (WARNING - date subject to change) Review of analog circuit concepts (EECE525 material)	Class notes
9	Current mirrors, sources and sinks Voltage references	Sect 20.1 Chap 21
10	Amplifiers (common source, drain, and gate, active loads) Differential amplifiers	Section 22.1, 22.2 Sect 24.1, 24.3
11	Class project description Class project circuits - counters, VCOs, phase detectors, summers, mixers...	Class notes Class notes
12	Placement and routing, probe pads, and test planning Project discussions	Chap 15, class notes
13	Additional topics - opamps, OTAs, and comparators Project discussions	Sects 25.1, 25.2, 26.1
14	Additional topics - Dynamic logic, RAM/ROM Project discussions	Chap 14, Chap 17
15	Additional topics - BiCMOS, SOI, and GaAs processes Project discussions	Chap 16, class notes
16	Additional topics - Gate Array/Std cells/PLD IC design methods Project discussions	Class notes
17	<u>Final Exam</u>	